Computer Architecture Lec 5b

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(Partly taken from Dr. Alon Schclar slides)

Based on slides by:
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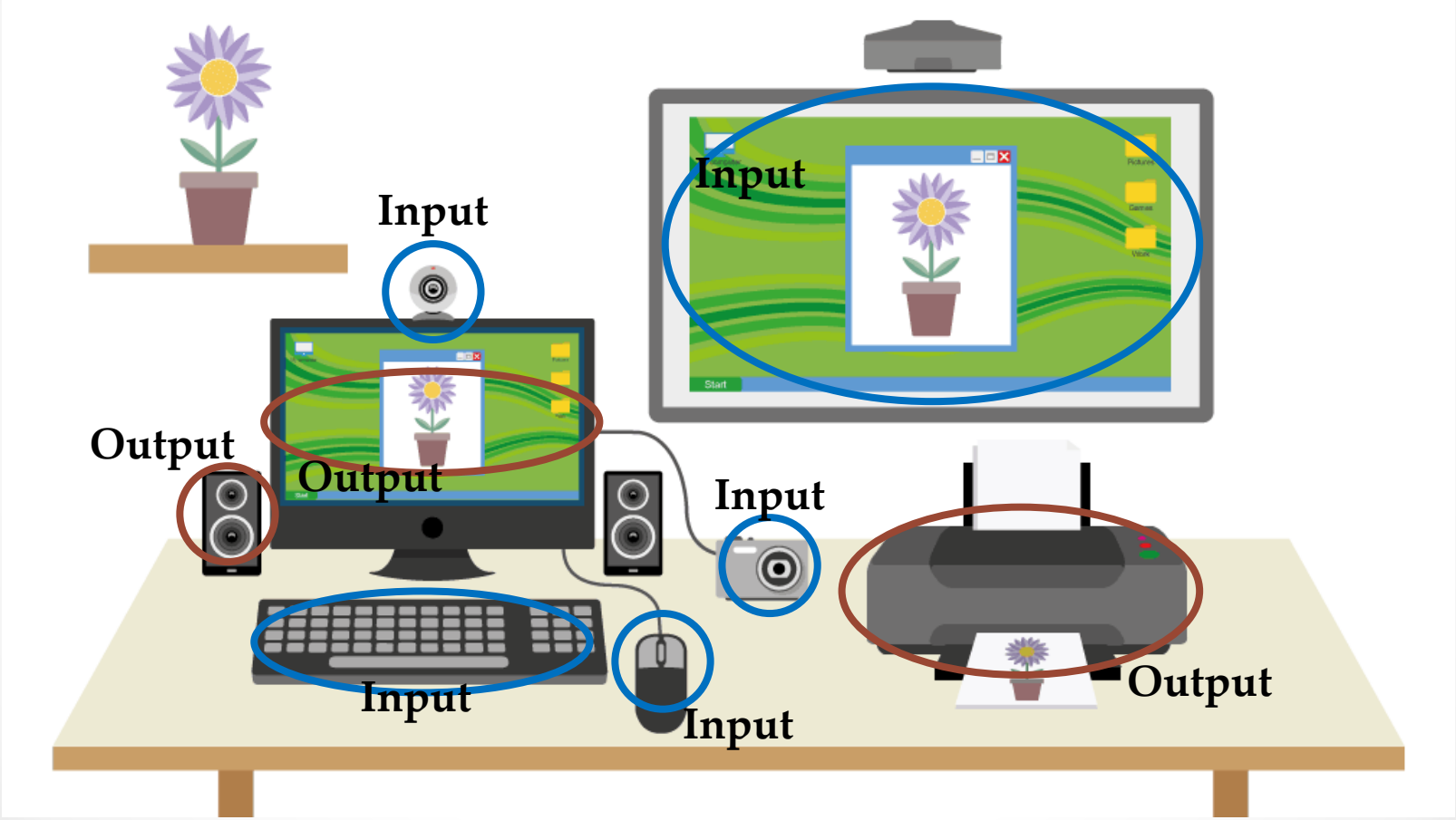
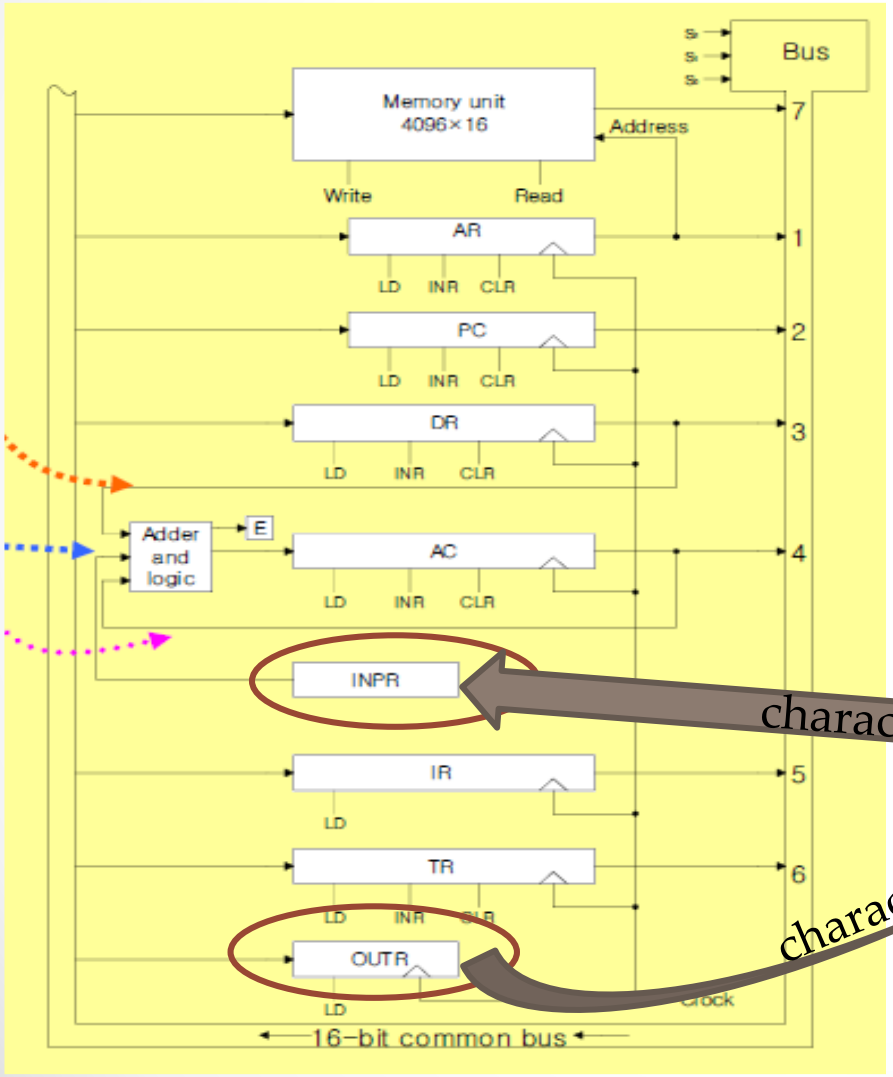
Taken from: **M. Mano/Computer Design and Architecture 3rd Ed.**

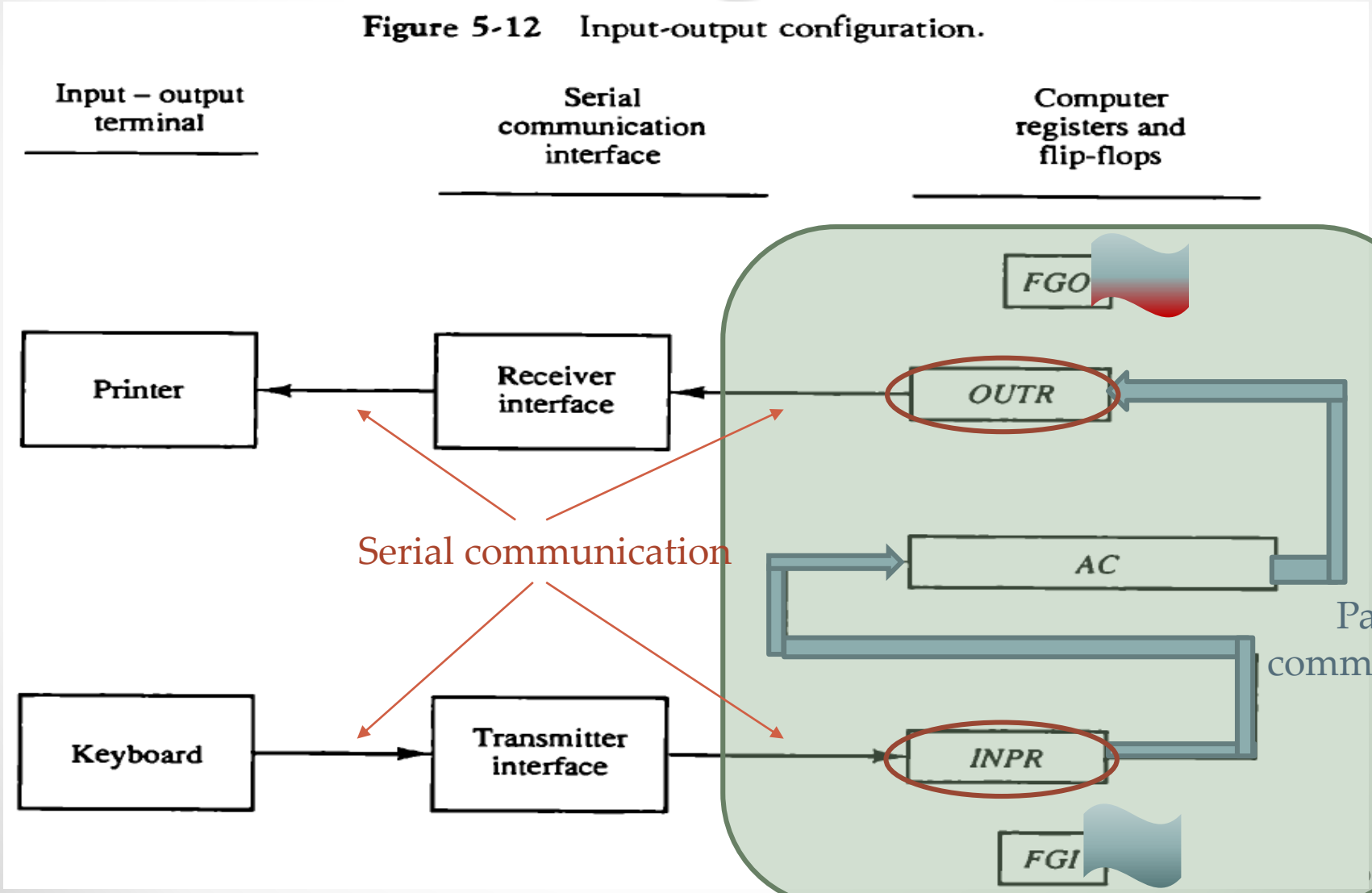
Input / Output



Our I/O Configuration

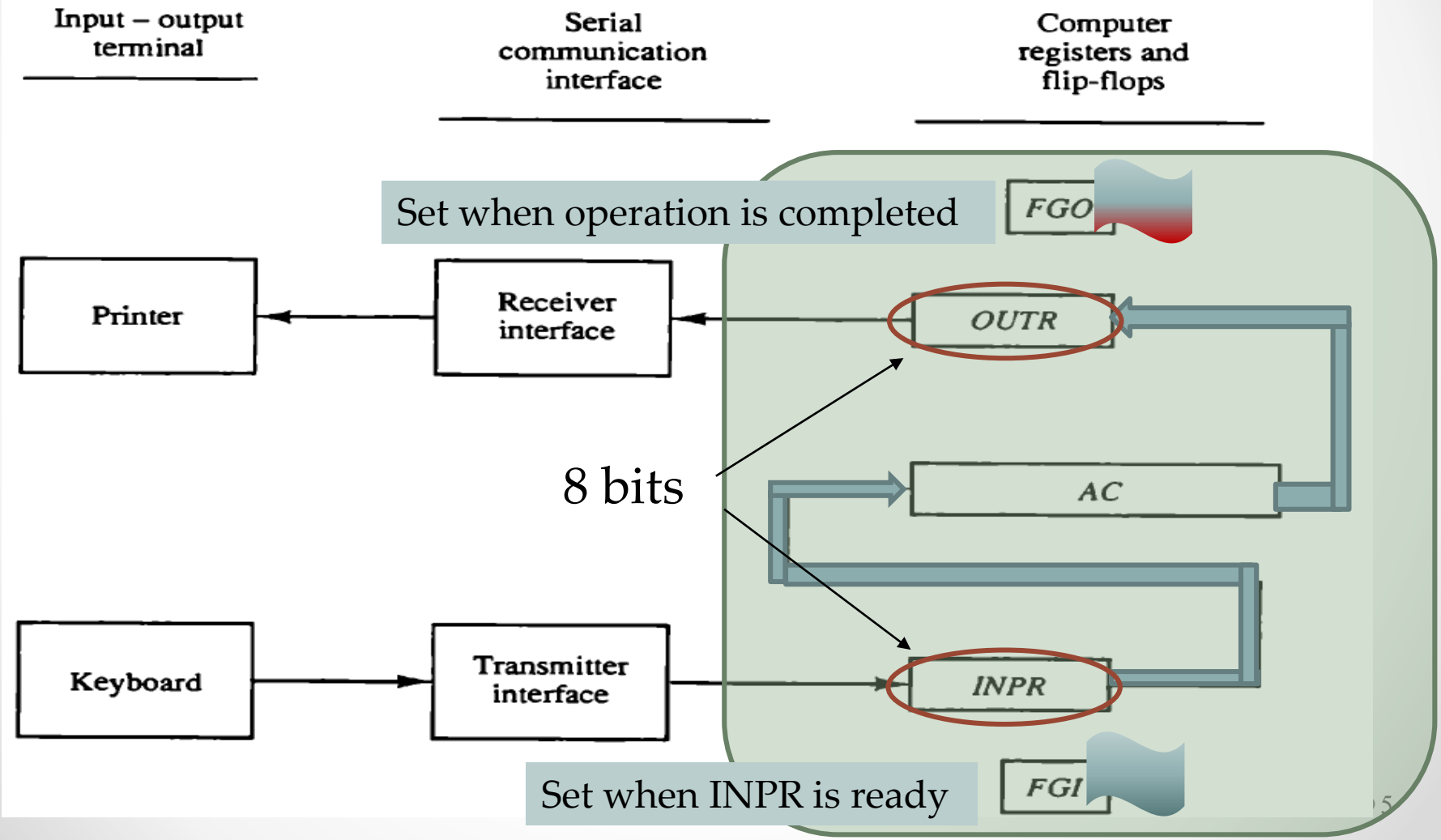


I/O Configuration

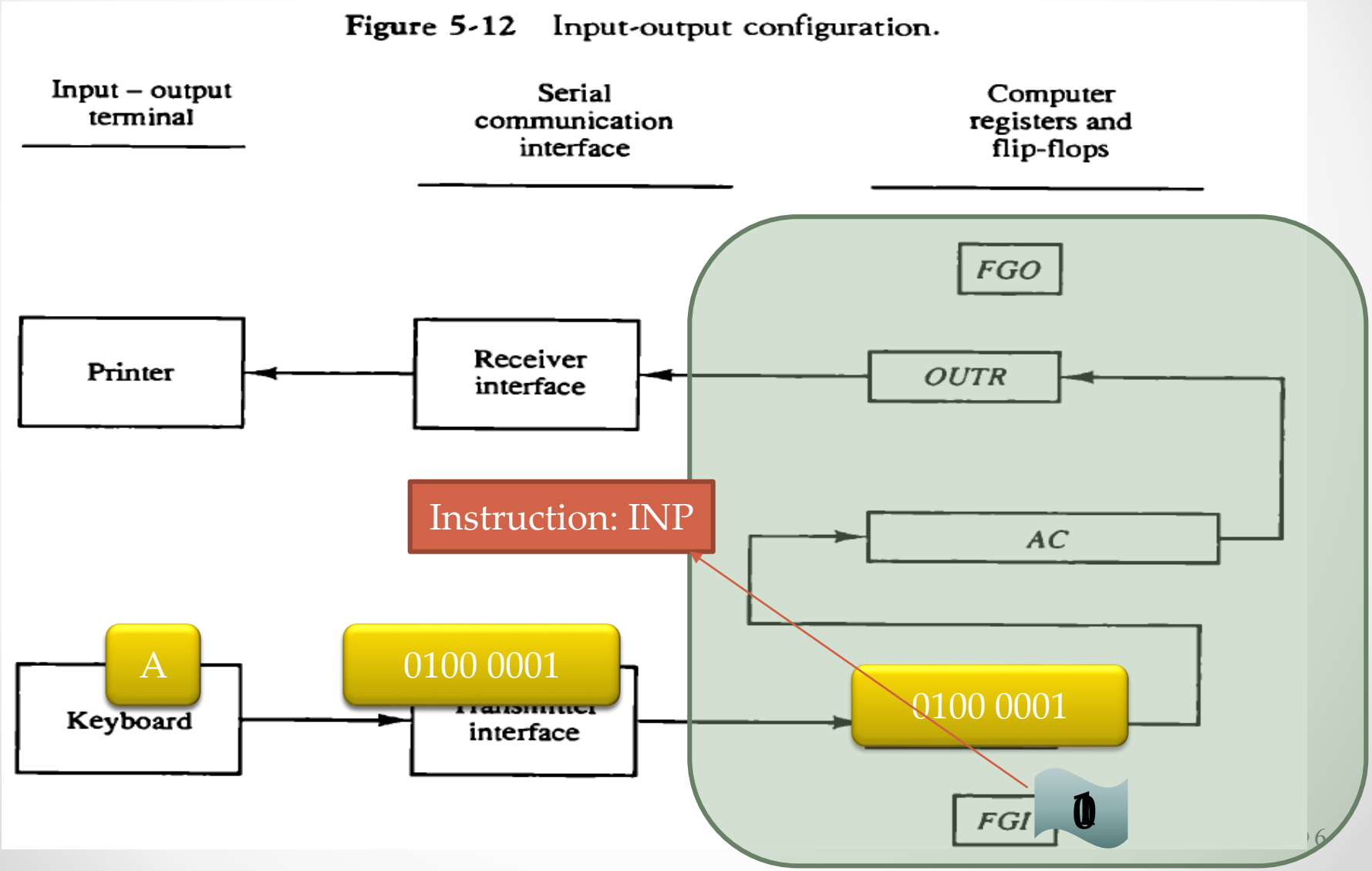


I/O Configuration

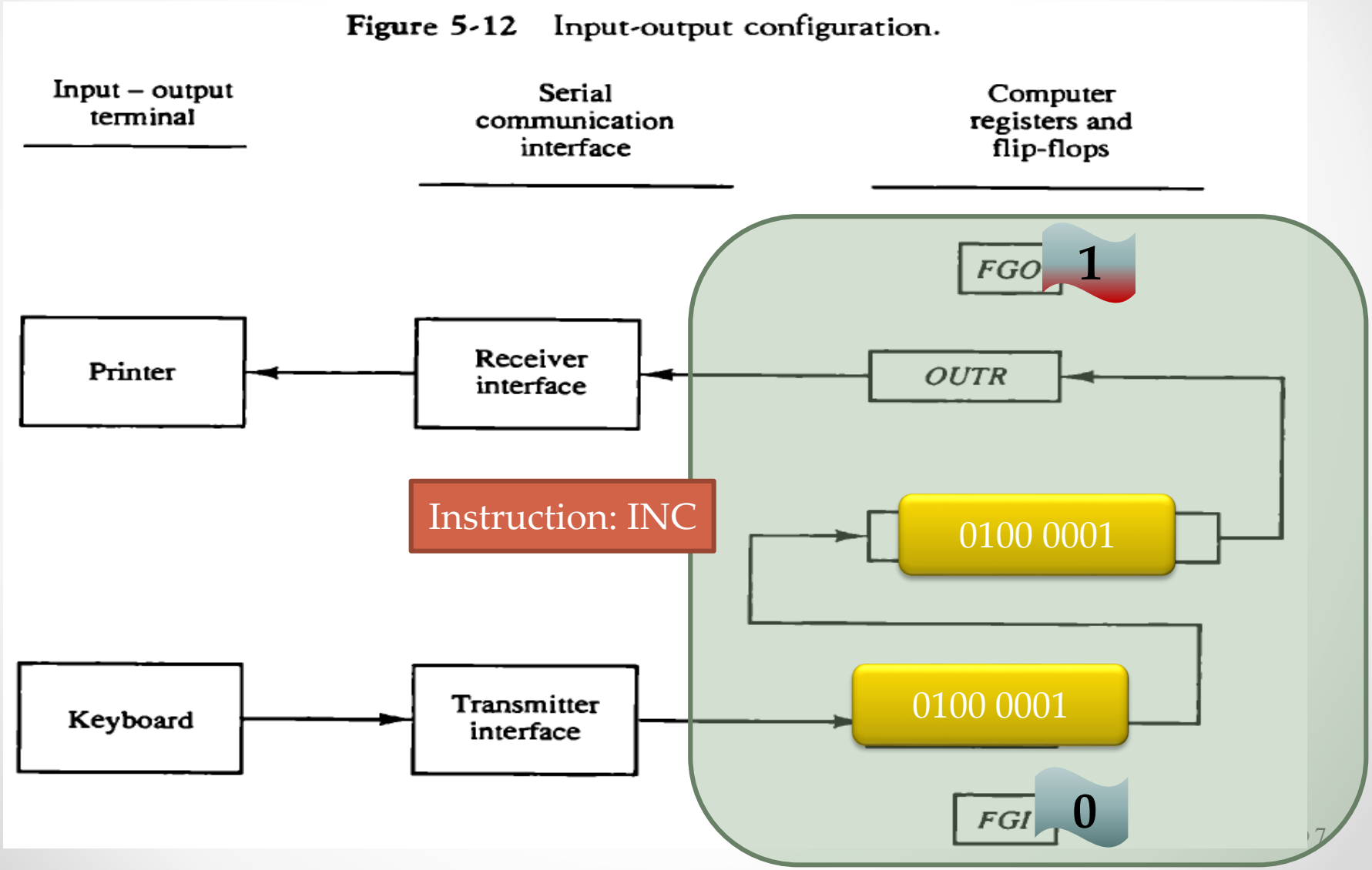
Figure 5-12 Input-output configuration.



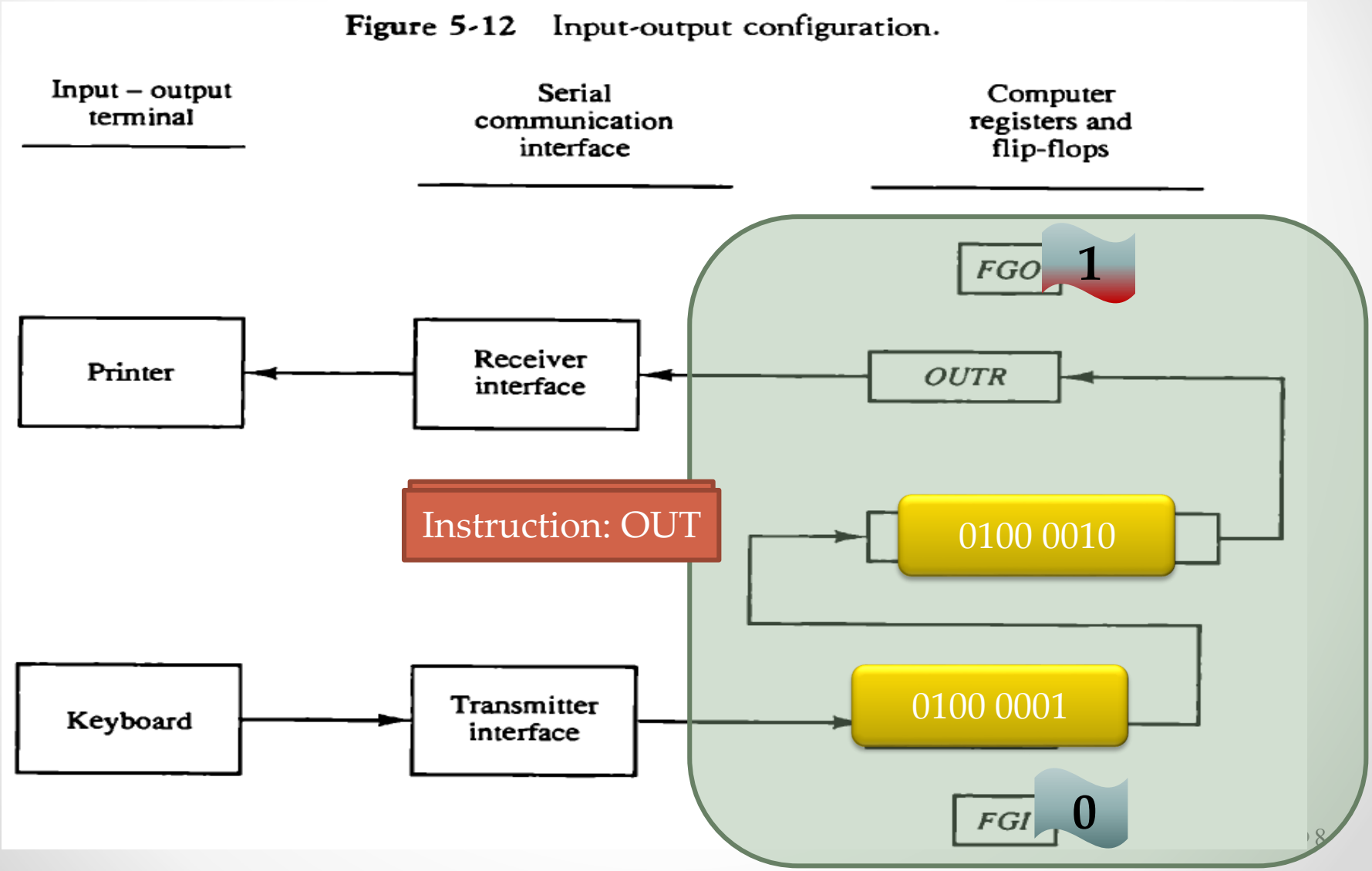
I/O Demonstration



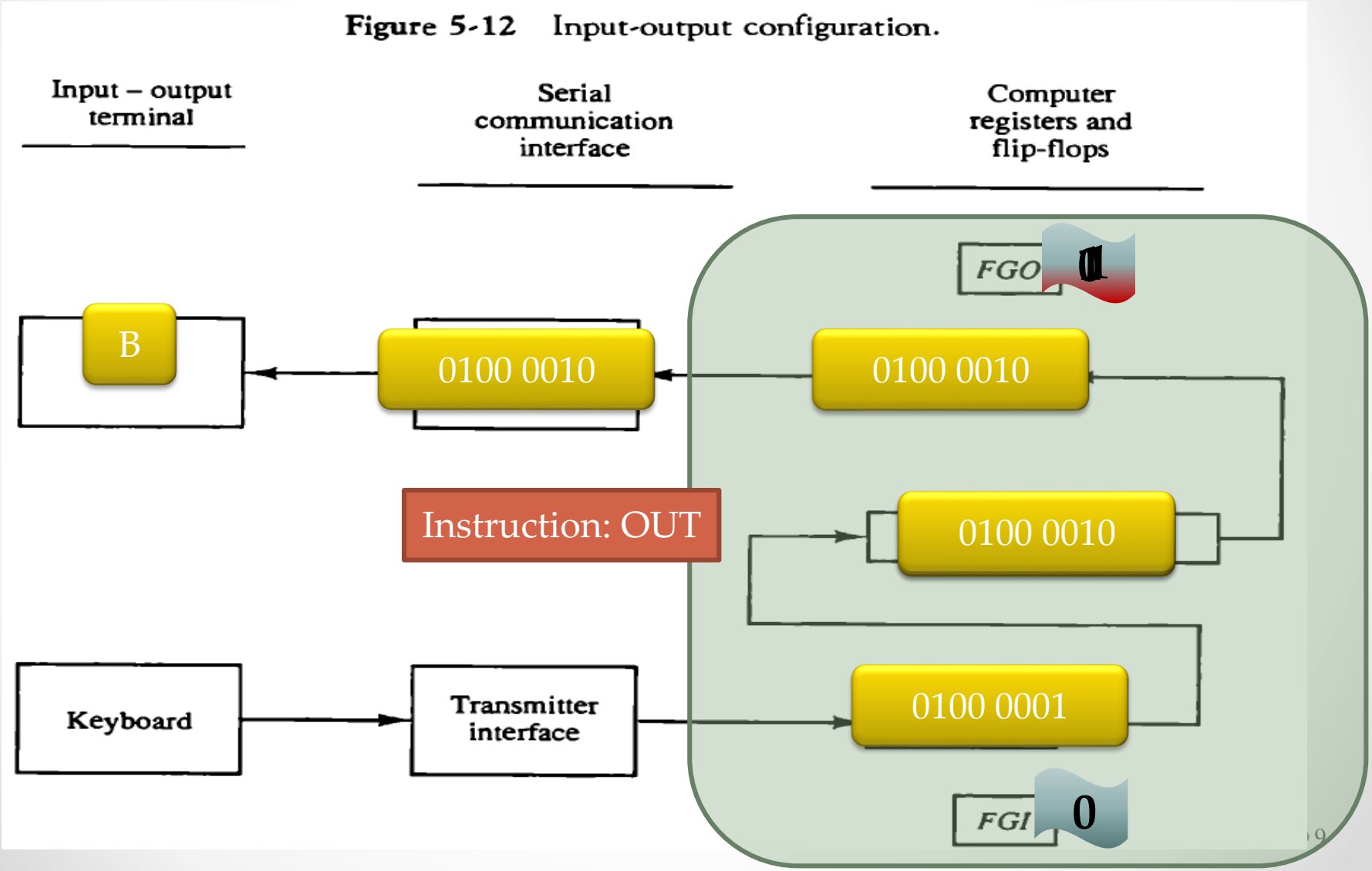
I/O Demonstration



I/O Demonstration



I/O Demonstration



The I/O Instructions

TABLE 5-5 Input-Output Instructions

$D_7IT_3 = p$ (common to all input–output instructions)
$IR(i) = B_i$ [bit in $IR(6\text{–}11)$ that specifies the instruction]

		p:	$SC \leftarrow 0$	Clear SC
F800	INP	pB_{11}:	$AC(0\text{–}7) \leftarrow INPR$, $FGI \leftarrow 0$	Input character
F400	OUT	pB_{10}:	$OUTR \leftarrow AC(0\text{–}7)$, $FGO \leftarrow 0$	Output character
F200	SKI	pB_9:	If $(FGI = 1)$ then $(PC \leftarrow PC + 1)$	Skip on input flag
F100	SKO	pB_8:	If $(FGO = 1)$ then $(PC \leftarrow PC + 1)$	Skip on output flag
F080	ION	pB_7:	$IEN \leftarrow 1$	Interrupt enable on
F040	IOF	pB_6:	$IEN \leftarrow 0$	Interrupt enable off

Determine Instruction Type

- 5-3 Computer Instruction
  - 3 Instruction Code Formats : *F*
    - Memory-reference instruction
      - » Opcode = 000 ~ 110
        - I=0 : 0xxx ~ 6xxx, I=1: 8xx

I=0 : Direct,
I=1 : Indirect

15	14	12	11	0
I	Opcode		Address	

I

- Register-reference instruction
  - » 7xxx (7800 ~ 7001) : CLA, C

15	14	12	11	0
0	1	1	1	Register Operation

- Input-Output instruction
  - » Fxxx(F800 ~ F040) : INP, O

15	14	12	11	0
1	1	1	1	I/O Operation

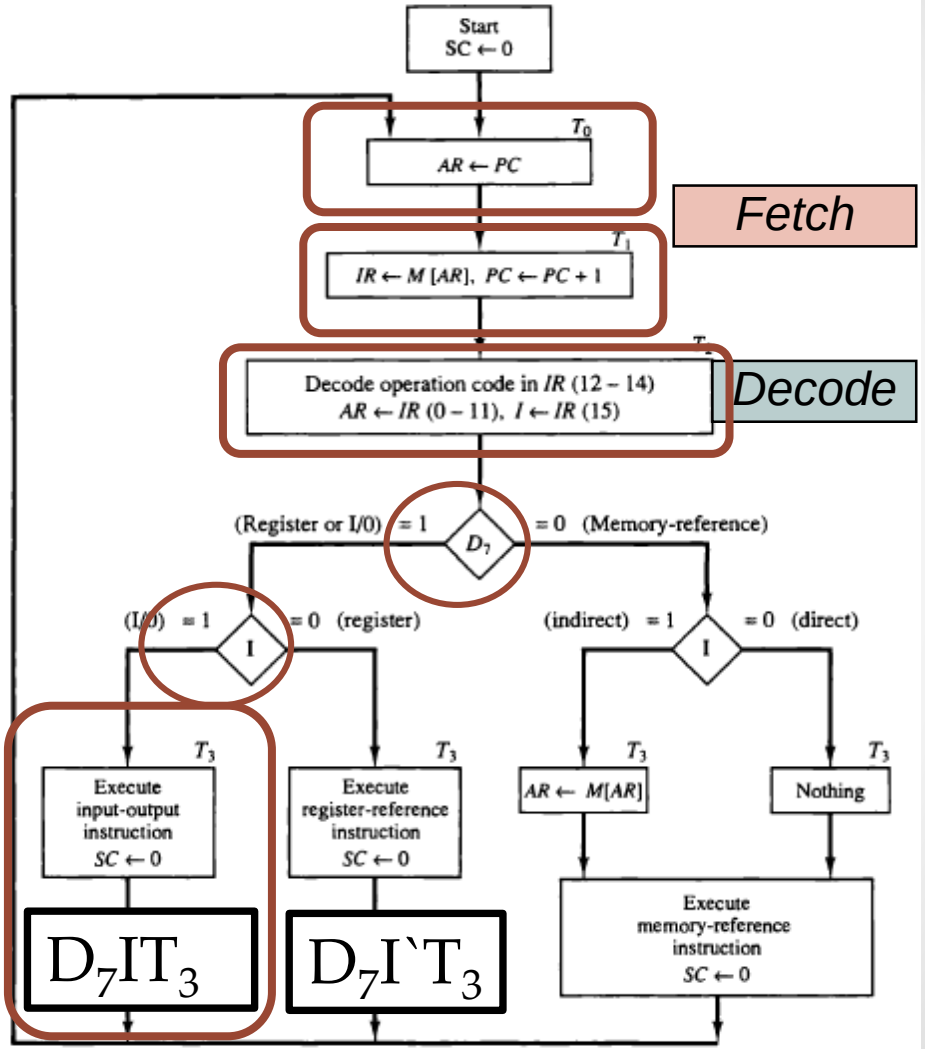
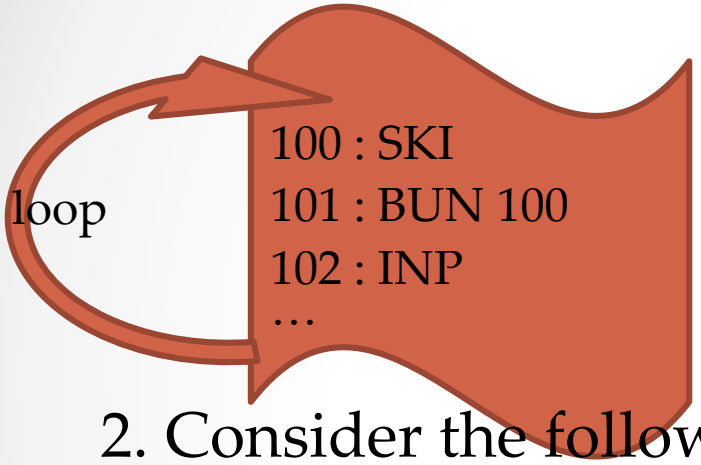


Figure 5-9 Flowchart for instruction cycle (initial configuration).

QUIZ1

Consider the following code:



1. Instruction 102 is performed when

_____

2. Consider the following:
   a. An instruction cycle takes 1μs (10^{-6} second)
   b. The I/O device can transfer information at maximum rate of 10 characters per second

On <u>maximum</u> rate transfer:

How many times FGI will be checked between two transfers? _____

The Interrupt

BUSY WAIT:

The computer is wasting time while checking the flag instead of doing some other useful processing task.

ALTERNATIVE:

The computer lets the external device inform when it is ready for the transfer.

Meanwhile, the computer can be busy with other tasks.

This mechanism is called: INTERRUPT

The Interrupt

- While **running** a program, the computer **does not check** the flags.
- When an I/O flag is set, the computer
  - Is **informed**
  - Is **momentarily interrupted** from proceeding with the current program
  - **Deviates momentarily** from what it is doing to take care of the I/O
  - **Resumes** program execution

Special procedure

Controlling The Interrupt Facility

- ***I*nterrupt *EN*able** flip-flop (IEN)
  - set to 1 via ***ION* instruction**
  - cleared to 0 by the ***IOF* instruction**
- When ***IEN*** is clear (**=0**)
  - the flags **cannot interrupt** the computer.
- When ***IEN*** is set (**=1**)
  - The computer **can be interrupted**.
- **ION, IOF allow** the programmer to **decide whether or not to** use the **interrupt** facility.

Flowchart for interrupt cycle

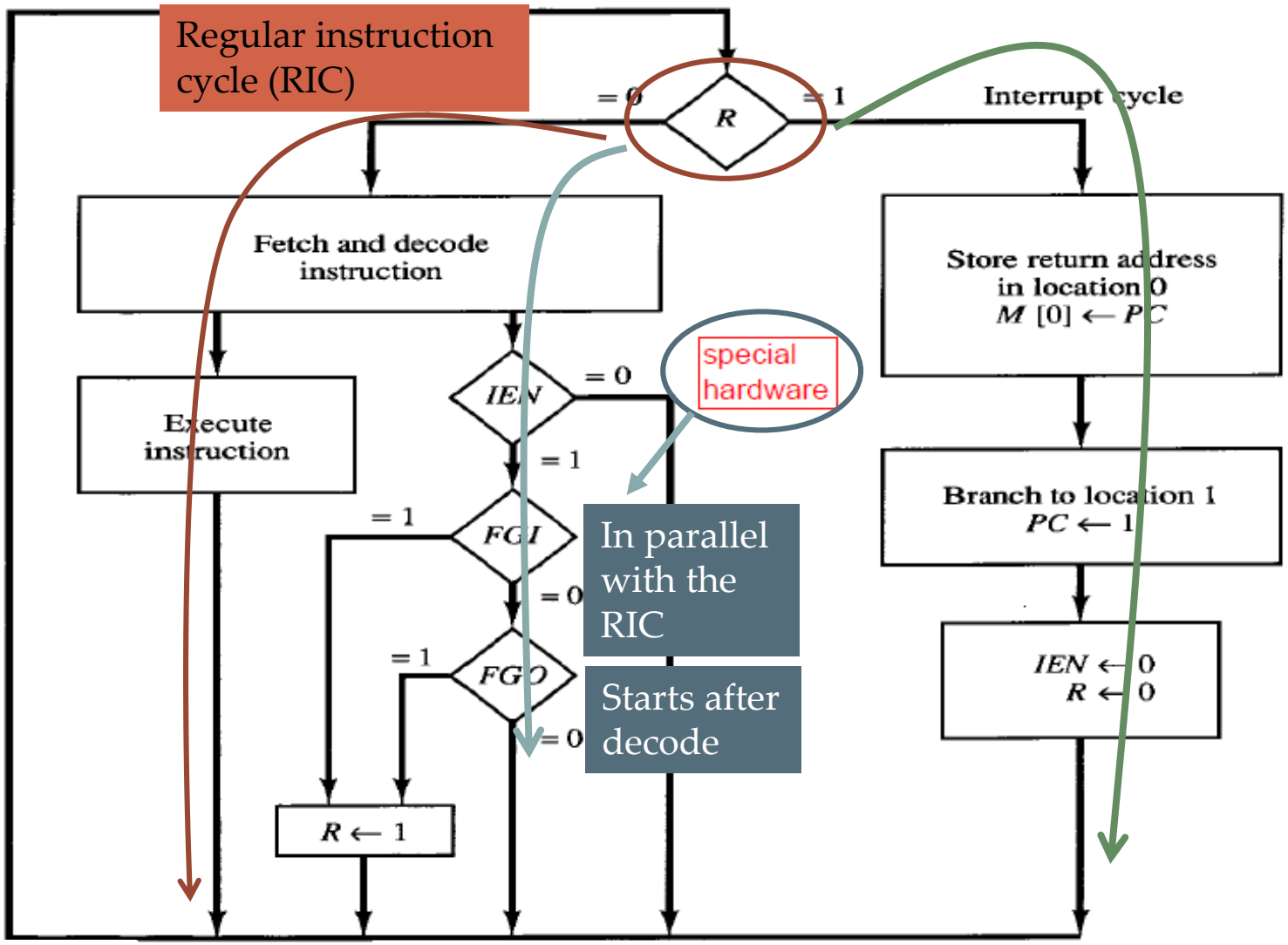


Figure 5-13 Flowchart for interrupt cycle.